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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/722,561	11/28/2003	Makoto Terui	OHG 147	4986

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EXAMINER	
WARREN, MATTHEW E	
ART UNIT	**PAPER NUMBER**
2815	

DATE MAILED: 06/01/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

EK

Office Action Summary	Application No.	Applicant(s)	
	10/722,561	TERUI, MAKOTO	
	Examiner	Art Unit	
	Matthew E. Warren	2815	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *07 March 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1 and 3-23* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,3-16,18,19 and 21-23* is/are rejected.

7)☒ Claim(s) *17 and 20* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *11/8/04*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

This Office Action is in response to the Amendment filed on March 7, 2005.

Claim Rejections - 35 USC § 112

The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

Claims 1-14 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the written description requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention. The amendments to the claims state that the semiconductor device comprises "at least one electrode pad which is formed on the circuit region; a first redistribution wiring which is disposed between the electrode pad and the first external terminal, and which electrically connects the electrode pad to the first external terminal, and a second redistribution wiring which is disposed between the electrode pad and the second terminal, and which connects the electrode pad to the second external terminal...." With these limitations, it seems that the one electrode pad has two redistribution wirings; one redistribution wiring is connected to the first external terminal and the second redistribution wiring is connected to the second external terminal. The drawings or specification do not disclose that one pad is connected to a first and second external terminal. The drawings only show (for example fig. 4) that one

pad (212) in the circuit region is connected to a first external terminal (222) and a second electrode pad (211) is connected to a second external terminal (232). For purposes of examination, the claims will be interpreted to mean that "there are two electrode pads formed on the circuit region, wherein a first redistribution wiring is disposed between the first electrode pad and the first external terminal, and which electrically connects the first electrode pad to the first external terminal, and a second redistribution wiring which is disposed between the second electrode pad and the second external terminal and which connects the second electrode pad to the second external terminal.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claims 1, 5, 8, 12-16, 18, and 19 are rejected under 35 U.S.C. 102(e) as being anticipated by Terui et al. (US Pub 2003/0189251 A1).

The applied reference has a common inventor with the instant application. Based upon the earlier effective U.S. filing date of the reference, it constitutes prior art under 35 U.S.C. 102(e). This rejection under 35 U.S.C. 102(e) might be overcome

either by a showing under 37 CFR 1.132 that any invention disclosed but not claimed in the reference was derived from the inventor of this application and is thus not the invention "by another," or by an appropriate showing under 37 CFR 1.131.

In re claim 1, as far as understood, Terui et al. (figs. 9-14) a semiconductor chip which has includes a circuit region (107a or 107b) and a wiring region (outside the circuit regions) which surrounds the circuit region; an integrated circuit which is formed in the circuit region; at least one electrode pad (103b) which is formed on the circuit region and which is connected to the integrated circuit'; at least one first external terminal (201) arranged over the circuit region'; at least one second external terminal (201 left side) arranged over the wiring region; a first redistribution wiring (105b middle) which is disposed between the electrode pad and the first external terminal and which electrically connects the electrode pad to the first external terminal; a second redistribution wiring (105b on the left side) which is disposed between the electrode pad and the second external terminals and which connects the electrode pad to the second external terminal; a passive element (1101 in fig. 14) which is disposed over the wiring region and which is connected to the second redistribution wiring; and a sealing film (203) which covers over the circuit region and the wiring region such that the first and second external terminals are exposed from the sealing film.

In re claim 5, Terui shows (fig. 14) that the passive element includes an inductor (1101).

In re claim 8, Terui shows (fig. 13) that the passive element is formed in a layer in which the second redistribution wiring is formed.

In re claim 12, Terui shows (figs. 9 and 10) that a plurality of electrode pads (103b) are formed along the boundary between the circuit region and the wiring region.

In re claims 13 and 14, Terui shows (fig. 10) a first or second post electrode (305) having an external terminal (201) provided on its top surface and a first or second redistribution wiring (111b) connected to its bottom surface.

In re claim 15, Terui shows (figs. 9-14) a semiconductor device, comprising: a semiconductor substrate which includes a first region that includes a plurality of circuit element connection pads (103b), and a second region that surrounds the first region; a plurality of first external terminals (201 in the center) which are arranged over the first region; a plurality of second external terminals (201 left) which are arranged over the second region; a plurality of first wiring structures (111b center) which are formed over the first region, and electrically and individually connect a plurality of the first external terminals and a first predetermined number of the circuit element connection pads; a plurality of second wiring structures (111 on the left) which are formed from the first region to the second region, and electrically and individually connect a plurality of the second external terminals and a second predetermined number of the circuit element connection pads; a passive element (1101 in figs. 14-16) which is disposed over the second region and which is electrically connected to one of the second wiring structures.

In re claims16 and 19, Terui shows (figs. 9-14) that each of the first wiring structures includes a first redistribution wiring layer (111b center) which is electrically and individually connected to one of the first predetermined number of the circuit

element connection pads (103b), and a first post electrode 305 center) which electrically and individually connects the first redistribution wiring layer and the one of the first external terminals (ball 201); each of the second wiring structures includes a second redistribution wiring layer (111b left) which is formed ranging from the first region (107a) to the second region and is electrically and individually connected to one of the circuit element connection pads (103b on the left), and a second post electrode (305 left) which electrically and individually connects the second redistribution wiring layer and one of the second external terminals (ball 201); and the passive element (1101 in the embodiments of figs. 14-16) is electrically connected to one of the second redistribution wiring layer.

In re claim 18, Terui shows (figs. 14-16) that the passive element is an inductor and has been placed in a route of the second redistribution wiring layer.

Claims 3, 4, 6, 7, 9-11, and 21-23 are rejected under 35 U.S.C. 103(a) as being unpatentable over Terui et al. (US Pub 2003/0189251 A1) as applied to claim 1 above, and further in view of Aoki (US Pub. 2002/0149086 A1).

In re claims 3, 4, 6, 7, and 9-11 Terui shows all of the elements of the claims except the passive element being a capacitor provided in the wiring region. Aoki shows (figs. 15A-15C) the device further comprising a passive element (L or C) which includes a capacitor or inductor, which is provided in the wiring region and which regulates the

electrical characteristics of the second redistribution wiring. The passive element may be a plurality of capacitors (C1 and C2) or inductors which are standardized or formed in an array so as to have the same size. In fig. 14, the passive element being a capacitor is formed in a layer in which a redistribution rewiring (4) is formed. In fig. 11, the passive element being a capacitor, is formed in a layer that lies beneath layer in which a redistribution wiring (8) formed. In fig. 15B, the redistribution wiring comprises a wiring part (connected to 10) that connects the electrode pad to the passive element and another wiring part that connects the passive element to the second external terminal (6). The device includes a passive element electrode pad (12-2), in which the passive element is connected to the wiring part (10) via the passive element electrode pad. The device further comprises (fig. 14) a first or second post electrode (6) having an external terminal (B) provided on its top surface and a first or second redistribution wiring (connected to electrode 2 or 5-2) connected to its bottom surface. With this configuration, a passive component can be formed in the wiring layers to provide an antenna or signal filtering. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the wiring of Terui by forming a capacitive passive element in the wiring layer as taught by Aoki to provide an antenna or signal filtering.

In re claims 21 and 22, Terui does not specifically show that the inductor has two passive element electrode pads. Aoki shows fig. (15A-15C) that the passive element that is connected to the redistribution wiring layer is an inductor (L) which has two passive element electrode pads (connected to wiring layer 10) connected at ends of the

inductor. The pads of the inductor are connected to the redistribution layer (10). The passive elements may be arranged in an array when combined with the routing array of Terui.

In re claim 23, the limitations are "product-by-process" limitations. A "product by process" claim limitation is directed to the product per se, no matter how actually made, In re Hirao, **190 USPQ 15 at 17**(footnote 3). See also in re Brown, **173 USPQ 685**: In re Luck, **177 USPQ 523**; In re Fessmann, **180 USPQ 324**: In re Avery, **186 USPQ 116** in re Wertheim, **191 USPQ 90** (**209 USPQ 254** does not deal with this issue); and In re Marosi et al, **218 USPQ 289** final product per se which must be determined in a "product by, all of" claim, and not the patentability of the process, and that an old or obvious product, whether claimed in "product by process" claims or not. Note that Applicant has the burden of proof in such cases, as the above case law makes clear.

"Even though product-by- process claims are limited by and defined by the process, determination of patentability is based upon the product itself. The patentability of a product does not depend on its method of production. If the product in product-by-process claim is the same as or obvious from a product of the prior art, the claim is unpatentable even though the prior product is made by a different process." In re Thorpe, 227 USPQ 964, 966 (Fed. Cir. 1985)(citations omitted).

Allowable Subject Matter

Claims 17 and 20 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Response to Arguments

Applicant's arguments with respect to claims 1-22 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Tahara et al. (US 2002/0017730) and Shimizu et al. (US 6,211,576 B1) also show semiconductor devices having efficient redistribution routing schemes.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Matthew E. Warren whose telephone number is (571) 272-1737. The examiner can normally be reached on Mon-Thur and alternating Fri 9:00-5:00pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Tom Thomas can be reached on (571) 272-1664. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

MEW
MEW
May 27, 2005

TOM THOMAS
SUPERVISORY PATENT EXAMINER